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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/662,093

09/12/2003

Jeffrey D. Gilbert

042390.P17020

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7590

07/25/2008

INTEL/BSTZ

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EXAMINER

CHERY, MARDOCHIEE

ART UNIT

PAPER NUMBER

2188

MAIL DATE

DELIVERY MODE

07/25/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/662,093

Applicant(s)

GILBERT ET AL.

Examiner

MARDOCHEE CHERY

Art Unit

2188

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 April 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-31 and 33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 11-30 is/are allowed.
- 6) ☒ Claim(s) 1,3-10,31,33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____
- Paper No(s)/Mail Date _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 18, 2008 has been entered.

Response to Amendment

2. This Office action is a reply to applicants' communication filed on April 18, 2008 in response to PTO Office Action mailed on April 3, 2008. Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

3. Claims 1 and 31 have been amended. Claims 1, 3-31, and 33 remain pending.

Response to Arguments

4. Applicant's arguments, see remarks filed February 28, 2008, with respect to claims 11-30 have been fully considered and are persuasive. The rejection of claims 11-30, under 35 U.S.C. 103 has been withdrawn. However, the rejection of claims 1, 3-10, 31, and 33 is maintained and claims 1, 3-10, 31, and 33 are further rejected under

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35 U.S.C. 112, first paragraph for the newly filed amendment finds no support in the original disclosure.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1, 3-10, 31 and 33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Particularly claims, 1 and 31 recite, "the cache line simultaneously having two cache coherency states". Though the original disclosure provides for for example, "a joint cache coherency state" in originally filed claims 11, 14, 18, 21, 24 and 28, wherein is recited "transitioning said first cache coherency state to a joint cache coherency state including said first cache coherency state for outer interfaces and an invalid state for inner interfaces", and in Fig. 2, and pages 7 , paragraph [0019] line 13 to page 8, paragraph [0021], line 9, such "joint cache coherency state" does not provide support for "the cache line simultaneously having two cache coherency states". Thus, claims 1, 3-10, 31 and 33 are rejected under 35 U.S.C. 112, first paragraph for new matter and further remain as rejected in the Office action mailed on November 1, 2007 as shown below.

Claim Rejections - 35 USC § 103.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1, 3-10, 31 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (6,629,268) in view of WO 00/52582 and further in view of Arimilli (2002/0129211).

As per claim 1, Arimilli (6,629,268) discloses an apparatus, comprising: a first interface [Fig.2; Bus Interface Unit 35]; a second interface not directly coupled to said first interface [Fig.2; Interface 18]; and a cache accessible from said first interface and said second interface [Fig.2; L2 cache, Bus Interface 35, Interface 19; col.8, lines 6-33].

However, Arimilli (268) does not specifically teach a cache containing a cache line with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface as required.

WO 00/52582 discloses a cache containing a cache line, the cache line having two cache coherency states, with a first cache coherency state when accessed from

said first interface and a second cache coherency state when accessed from said second interface [Fig. 1; page 11, ll 16-32; page 12, ll 21-27; Fig. 3; Page 12] to increase the performance capability of processor systems while ensuring that the cache memory block is not read unnecessarily (page 1, ll 1-5; page 11, ll 18-23).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Arimilli (268) to include a cache containing a cache line with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface since this would have increased the performance capability of processor systems while ensuring that the cache memory block is not read unnecessarily (page 1, ll 1-5; page 11, ll 18-23) as taught by WO 00/52582.

Arimilli (268) and WO disclose the claimed invention as discussed above in the previous paragraphs. However, Arimilli (268) and WO do not specifically teach the first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor as required by the claims.

Arimilli (2002/0129211) discloses the first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor [par. 10] to resolve conflicts between requests to modify a cache line (par. 2).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Arimilli (268) and WO to include the first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor because this would have resolved conflicts between requests to modify a cache line (par. 2).

As per claim 31, the rationale in the rejection of claim 1 is herein incorporated. Arimilli (268) further discloses a bus bridge to a third interface [Fig.1]; and an input-output device coupled to a third interface [Fig.3].

As per claim 3, Arimilli (211) discloses a second cache coherency state is to reduce snoop transactions on said second interface [par. 5].

As per claim 4, Arimilli (211) discloses said first cache coherency state is exclusive and said second cache coherency state is shared [pars. 6, 24 and 36].

As per claim 5, Arimilli (211) discloses first cache coherency state is modified and said second cache coherency state is shared [par. 8].

As per claim 6, Arimilli (211) discloses second cache coherency state supports speculative invalidation [par. 6].

As per claim 7, Arimilli (211) discloses first cache coherency state is modified and said second cache coherency state is invalid [par. 7].

As per claim 8, Arimilli (211) discloses first cache coherency state is exclusive and said second cache coherency state is invalid [pars. 6 and 36].

As per claim 9, Arimilli (211) discloses the first cache coherency state is shared and said second cache coherency state is invalid [par. 7].

As per claim 10, Arimilli (211) discloses the second cache coherency state further supports explicit invalidation [pars. 7 and 10].

As per claim 33, the rationale in the rejection of claim 3 is herein incorporated.

Conclusion

9. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

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10. When responding to the Office action, Applicant is advised to clearly point out where support, with reference to page, line numbers, and figures, is found for any amendment made to the claims.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hyung S Sough/
Supervisory Patent Examiner, Art Unit 2188
07/21/08

July 21, 2008

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Mardochee Chery
Examiner
AU: 2188